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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,146	02/11/2004	Teruo Takizawa	118623	2436

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)
	10/775,146	TAKIZAWA, TERUO
	Examiner	**Art Unit**
	Jennifer M. Dolan	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *8 and 9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/11/04; 7/7/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-7 in the reply filed on 9/9/05 is acknowledged. The traversal is on the grounds that a thorough search of the subject matter of any group of claims would encompass a search for the subject matter of the remaining claims, and hence, examination of the entire application can be made without burden. This is not found persuasive because claims 8 (through product-by process analysis) and 9 read on semiconductor devices having the specified structure formed by any methods, including those vastly different from the method set forth in claims 1-7. For example, claims 1-7 are drawn to a method wherein a strained silicon layer on an insulating layer is provided by forming an overlying strain-inducing layer, and then annealing to alter the lattice of the single crystal layer. Claims 8 and 9, however, read on vastly different methods, such as using a layer transfer of a strained silicon layer from a donor wafer for forming the strained SOI layer. Hence, these inventions would not be encompassed by the same search, and the same references would not necessarily read on the claimed inventions of both Group I and Group II.

The requirement is still deemed proper and is therefore made FINAL.

Claims 8 and 9 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 3 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 3 requires the provision of a single crystal silicon layer on the strain-inducing layer. In combination with the limitations of claim 1, claim 3 thus requires a structure including a single crystal silicon layer, a strain-inducing semiconductor layer on the single crystal silicon layer, and another single crystal silicon layer formed on the strain-inducing layer. There is no supporting disclosure in the specification for this claimed structure, there is no indication of how or whether a single crystal layer formed on top of the strain-inducing layer might affect the defect density of the structure, and there are no teachings of the thickness required for such an overlying layer to prevent defects. Furthermore, as the specification and as claim 1 establish, the strain-inducing layer and hence, any overlying layers, are removed from the substrate, which makes it unclear exactly how a single crystal layer overlying the strain-inducing layer functions or precisely what purpose such a layer might serve.

For the purpose of examination, it is assumed that the structure includes a strained single crystal silicon layer with a strain-inducing layer formed thereon, wherein the strained single crystal silicon layer has a thickness such that no defect occurs in the strain-inducing layer (based upon page 7, lines 4-17 of the specification).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,774,015 to Cohen et al.

Regarding claim 1, Cohen discloses a method of manufacturing a semiconductor device (see column 1, lines 14-30) comprising: providing a substrate (160) having an insulating layer (150) and a single crystal silicon layer (100; column 4, lines 25-35) formed on the insulating layer (figure 1); forming a strain-inducing layer (110) on the single crystal silicon layer (figure 2; column 4, lines 44-46), the strain inducing layer having a different lattice constant than the single crystal layer (relaxed SiGe inherently has a different lattice constant than relaxed Si; also see column 3, lines 17-21); changing the single crystal silicon layer into a strained silicon layer by matching a lattice of the single crystal silicon layer with a lattice of the strain-inducing layer (see column 3, lines 22-35; column 5, lines 8-60; figure 6); and removing the strain-inducing semiconductor layer (figure 7; column 3, lines 35-37; column 5, lines 55-67).

Regarding claim 2, Cohen teaches that the step of forming strained silicon layer is performed using an annealing process (see column 5, lines 30-45).

Regarding claim 4, Cohen teaches that the strain-inducing layer is SiGe (see column 3, lines 1-38).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3 and 7 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Cohen et al.

Regarding claim 3, Cohen discloses that the single crystal layer is formed having a thickness substantially similar to the range of thicknesses disclosed by the applicant (column 4, lines 35-42), and hence, it is considered to have identical defect prevention properties. Cohen further teaches that the strained silicon has very low defect densities (column 6, lines 3-10), but does not indicate whether these defects are "caused" by or related to the thickness of the single crystal silicon layer, or whether the defect density is the artifact of some other process (i.e., the SOI deposition process, SIMOX, etc.). Since Cohen specifically does show a silicon layer having the same thickness as that disclosed by the applicant and additionally having a very low defect density, Cohen is considered to anticipate claim 3.

Assuming arguendo, Cohen does not have a sufficiently thin Si layer to prevent defect formation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specifically select a sufficiently small silicon layer thickness to minimize or prevent defect formation in the method of Cohen. The rationale is as follows: A person having ordinary

skill in the art would have been motivated to select a thin Si layer, because Cohen specifically teaches that the layer should be between 2-50 nm, and that selection of a thin layer allows for greater strain compensation without sacrificing crystal quality (see Cohen, column 4, lines 35-43).

Regarding claim 7, Cohen discloses an annealing process (column 5, lines 30-45). An annealing process is inherently and definitively understood to include a heat treatment, wherein the wafer is heated to the anneal temperature, annealed at the anneal temperature, and cooled to a temperature lower than the anneal temperature. Hence, Cohen would be understood by a person having ordinary skill in the art to meet the limitations of claim 7.

Cohen, however, does not explicitly teach the temperature increase and decrease steps as claimed.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the annealing process of Cohen includes a temperature increase, a constant temperature step, and a temperature decrease step. The rationale is as follows: A person having ordinary skill in the art would expect such steps to be present in an annealing process, because annealing by definition suggests a process wherein the temperature of a sample is raised for a set time (see the provided New Penguin Dictionary of Science definition). Since it is extremely common for semiconductor samples to be worked upon at room temperature, an annealing process must then inherently include a step of raising the sample temperature from room temperature to the anneal temperature, a step of annealing at the anneal temperature, and a step of cooling the sample down to room temperature.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen in view of U.S. Patent No. 6,200,866 to Ma et al.

Cohen teaches removal of the SiGe layer through wet-etching (column 5, lines 55-67), but does not specifically teach the use of a mixed acid of hydrofluoric acid and nitric acid.

Ma teaches selective removal of SiGe over Si by a mixture including hydrofluoric acid and nitric acid (see column 5, lines 35-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Cohen by using the SiGe etchant taught by Ma. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the etchant taught by Ma, because Ma shows that the HF/nitric etchant is highly etch selective of SiGe with respect to Si, and thus could effectively remove the SiGe layer in Cohen without unduly etching or removing the underlying strained Si layer (see Ma, column 5, lines 35-50).

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen et al. in view of U.S. Patent No. 6,750,486 to Sugawara et al.

Cohen is silent as to the method of SiGe deposition.

Sugawara teaches that SiGe layers are commonly deposited using MBE or ultrahigh vacuum CVD (column 1, lines 30-52).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to specify that the SiGe layer of Cohen be formed using the deposition methods taught by Sugawara. The rationale is as follows: A person having ordinary skill in the art would have

been motivated to use MBE or UHV-CVD for SiGe formation, because Sugawara shows that such methods are known in the art as suitable for forming high quality SiGe layers substantially similar to the layer required by Cohen (see Sugawara, column 1, lines 30-52). Since Cohen only suggests that the SiGe layer is formed by methods known in the art, it is reasonable and expected for a person having ordinary skill in the art to turn to references, such as Sugawara, in order to ascertain such known and suitable methods. It has further been held that "the selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945), and that "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. Also see MPEP § 2144.07.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent Publication No.2002/0140031 to Rim discloses an alternate method for forming strained SOI substrates.

The New Penguin Dictionary of Science, M.J. Clugston, 1998, definition for annealing – establishes that annealing is considered to include a step of heating, a step of holding at a fixed temperature for a time, and then a step of cooling.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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